DATA SHEET

GPEL3101A

Advanced ELA SOC Solution

Preliminary

Mar 12, 2013

Version 0.3

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ADVANCED ELA SOC SOLUTION

1. GENERAL DESCRIPTION

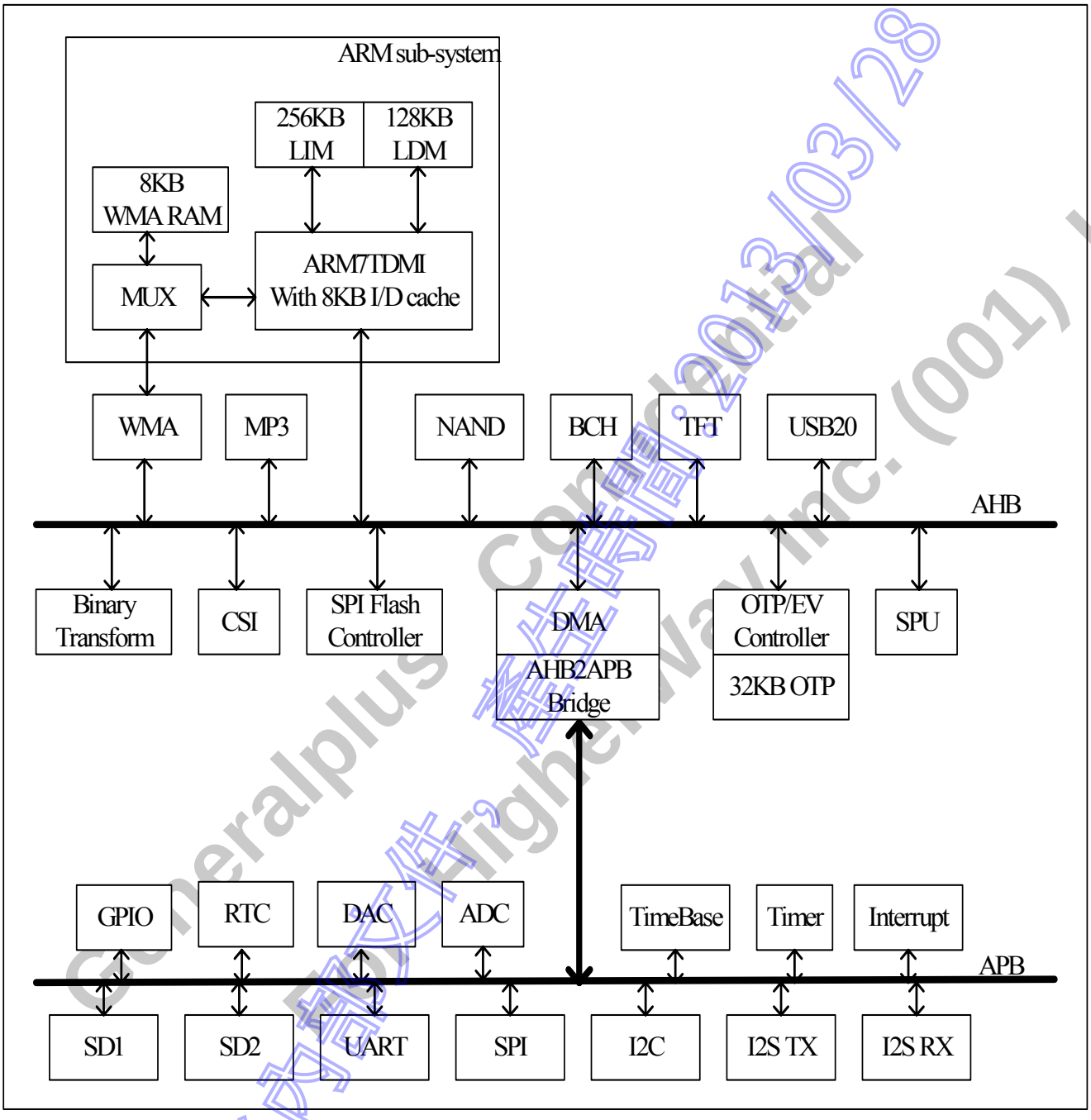
The Generalplus GPEL3101A, a highly integrated SoC (System-on-a-Chip), offers a great cost-effective and high performance ratio solution for ELA applications. It is embedded the ARM7TDMI with 8K-byte unified ID-cache and many tremendous features such binary transform engine for sensor input, SPI Flash controller on which CPU can run program directly , WMA accelerator, TFT-LCD interface, CMOS sensor interface, 60-bit BCH and Randomizer for MLC/TLC NAND Flash, UART interface which support smart card interface(ISO7816), 4-channel DMA controller, 6-channel 16-bit timers, RTC, two SD/MMC card interfaces, USB 2.0 mini-host/device, interrupt controller, SPI (master/slave) controller, 8-channel sound processing unit (SPU), programmable I/O ports, stereo 16-bit DAC for audio playback, 0.5W class AB mono audio amplifier, 8-channel 12-bit ADC, MIC, PLL, I2S TX/RX for external sigma-delta CODEC, 32K-byte OTP with EV mode, power control macro and 136K-byte embedded SRAM when WMA is disable.

With a complete set of common system peripherals, the GPEL3101A chip minimizes overall system cost and no additional component needs to be added. Not only does GPEL3101A feature the high-speed performance, but it is also a cost-effective system and the most important - compatible with all ARM based programs.

2. FEATURES

- ARM7TDMI CPU with 8KB unified ID-cache, embedded JTAG ICE, and working frequency up to 96MHz.
- Up to 136KB SRAM for local data buffer when WMA is disable. There is a dedicated 128KB internal SRAM if WMA is enable.
- 32KB OTP with EV mode
- SPI Flash controller which CPU can run program directly on it. Supports 1-bit/2-bit/4-bit IO mode both on STR and DTR. 2 SPI Flash are allowed in serial or parallel manner.
- WMA accelerator
- Video-in & CMOS sensor interface and CCIR601/CCIR656 standard supported.
- Binary transform engine for sensor input.
- Four-channel DMA controller.
- TFT-LCD controller.
  - UPS051. (serial RGB)
  - UPS052. (serial RGB dummy)
  - I80 (8-bit system bus) I/F type.
  - CCIR601/CCIR656.
- Interrupt Controller.
- Universal Serial Bus (USB) 2.0 high/full speed compliance device and USB mini-host with built-in transceiver. Support Bulk IN/OUT, Audio ISO IN/OUT, Video ISO IN and Interrupt IN transactions.
- BCH 60-bit/1K and Randomizer for MLT/TLC NAND Flash
- 8-channel sound processing unit (SPU). Each channel in this SPU can do ADPCM/PCM decode, volume multiply and left/right channel mute control.
- Watchdog timer.
- Six 16-bit timers/counters.
- Two SD/ SDHC/ SDIO/ MMC card interfaces.
- SPI (master/slave) interface with data rate up to 24Mbps.
- UART (asynchronous serial I/O) interface with baud rate up to 1.8432Mbps and 115.2Kbps. The UART interface can be configured as smart card interface(ISO7816)
- 42 Programmable general I/O ports (GPIO) with pull-high/low control.
- Built-in Power macro for power on/off controller and a 4.2V to 3.3V LDO and a 3.3V to 1.2V LDO.
- Dedicated 4.2V to 3.3V LDO for ADC/DAC.
- Real-time clock (RTC) with independent power supply.
- 216MHz PLL, range from 24MHz to 216MHz with 6MHz step
- 16-bit stereo DAC (2-channel) for audio playback.
- 0.5W class AB mono audio amplifier
- 12-bit ADC with 2 line-in channels and 2 internal channels for battery and 1.2V measurement.
- MIC with PGA. (Programmable Gain Amplifier)
- I2S TX/RX for external sigma-delta CODEC

3. BLOCK DIAGRAM



4. SIGNAL DESCRIPTIONS

LQFP64

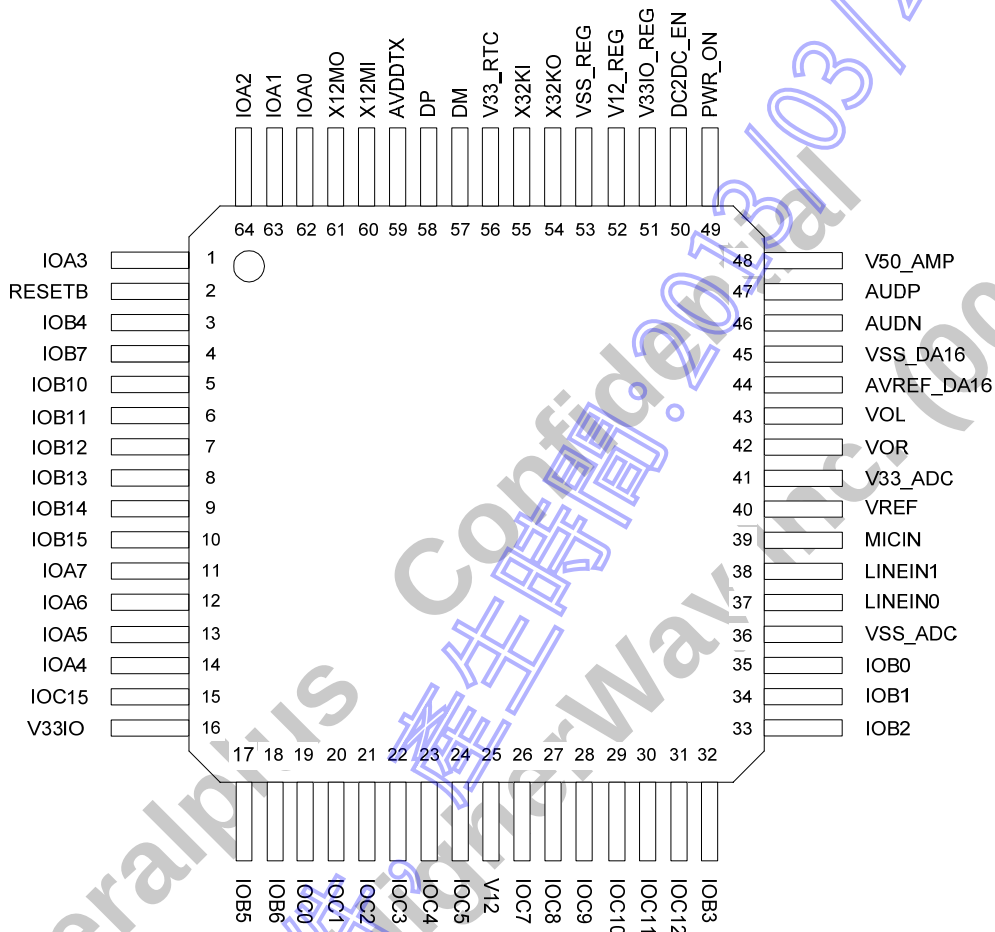
PKG No	Pin No	Name	Group	Type	Normal Function Description	GPIO Group
2	1	RESETB	System	I/O	Active low external reset.	
3	2	IOB4	CSI	I/O	CSI HSYNC	
4	3	IOB7	CSI	I/O	CSI VSYNC	
5	8	IOB10	CSI	I/O	CSI Data[2]	
6	9	IOB11	CSI	I/O	CSI Data[3]	
7	10	IOB12	CSI	I/O	CSI Data[4]	
8	11	IOB13	CSI	I/O	CSI Data[5]	
9	12	IOB14	CSI	I/O	CSI Data[6]	
10	13	IOB15	CSI	I/O	CSI Data[7]	
11	14	IOA7	TFT/NAND/SD2	I/O	TFT Data[4]/NAND Data[7]/SD2 CLK	
12	15	IOA6	TFT/NAND/SD2	I/O	TFT Data[4]/NAND Data[6]/SD2 CMD	
13	16	IOA5	TFT/NAND	I/O	TFT Data[4]/NAND Data[5]	
14	17	IOA4	TFT/NAND/SPIF	I/O	TFT Data[4]/NAND Data[4]/SPI Flash Data3	
15	24	IOC15	CSI	I/O	CSI Clock output to sensor	
16	25	V33IO	Digital PWR	P	3.3V digital power	
17	27	IOB5	I2C	I/O	I2C SCL	
18	28	IOB6	I2C	I/O	I2C SDA	
19	29	IOC0	SPI	I/O	SPI CSB	
20	30	IOC1	SPI	I/O	SPI CLK	
21	31	IOC2	SPI	I/O	SPI TX	
22	32	IOC3	SPI	I/O	SPI RX	
23	33	IOC4	SD/UART	I/O	SD CMD/UART TX	
24	34	IOC5	SD/UART	I/O	SD CLK/UART RX	
25	36	V12	Digital PWR	P	1.2V digital power	
26	46	IOC7	SD	I/O	SD DAT0	
27	47	IOC8	SD	I/O	SD DAT1	
28	48	IOC9	SD/TFT	I/O	SD DAT2/TFT CSB	
29	49	IOC10	CSI	I/O	CSI Clock input from sensor	
30	50	IOC11	NAND	I/O	NAND RDY	
31	51	IOC12	NAND	I/O	NAND CSB	
32	56	IOB3	TFT/NAND/SD2	I/O	TFT WEB/NAND WEB/SD2 DAT2	
33	57	IOB2	NAND/SD2	I/O	NAND OEB/SD2 DAT1	
34	58	IOB1	TFT/NAND/SD2	I/O	TFT RS/NAND CLE/SD2 DAT0	
35	59	IOB0	TFT/NAND/SD2	I/O	TFT OEB/NAND ALE/SD2 DAT3	
36	61	VSS_ADC	ADC	P	ADC ground	
37	62	LINEIN0	ADC	AI,I/O	ADC LINEIN0/GPIO	IOD0
38	63	LINEIN1	ADC	AI,I/O	ADC LINEIN1/GPIO	IOD1
39	68	MICIN	ADC	AI,I/O	ADC MICIN/GPIO	IOD6
40	69	VREF	ADC	AI,I/O	ADC VREF/GPIO	IOD7
41	70	V33_ADC	ADC	P	ADC 3.3V power	
42	72	VOR	ADAC	AO,O	Audio DAC right channel output/I2S TX	IOD12
43	73	VOL	ADAC	AO,O	Audio DAC left channel output/I2S BCK	IOD11
44	74	AVREF_DA16	ADAC	AIO	Audio DAC VREF/I2S LR	IOD10

PKG No	Pin No	Name	Group	Type	Normal Function Description	GPIO Group
45	75	VSS_DA16	ADAC	I/O	Audio DAC ground	
46	78	AUDN	AMP	AO	Audio amplifier push-pull N-output	
47	80	AUDP	AMP	AO	Audio amplifier push-pull P-output	
48	82	V50_AMP	AMP	I/O	Audio amplifier power	
49	86	PWR_ON	POWER	I	External power key input	
50	87	DC2DC_EN	POWER	O	DC2DC enable to external DC2DC	
51	88	V33IO_REG	POWER	P	LDO 3.3V output	
52	92	V12_REG	POWER	P	LDO 1.2V output	
53	95	VSS_REG	POWER	P	Power macro/LDO ground	
54	96	X32KO	RTC	AO	32768Hz crystal output pin	
55	97	X32KI	RTC	AI	32768Hz crystal input pin	
56	98	V33_RTC	RTC	P	RTC power	
57	101	DM	USB	AIO	USB DM	
58	102	DP	USB	AIO	USB DP	
59	103	AVDDTX	USB	P	USB 3.3V power	
60	106	X12MI	PLL	I	12MHz crystal input pin	
61	107	X12MO	PLL	O	12MHz crystal output pin	
62	109	IOA0	TFT/NAND/SPIF	P	TFT Data[0]/NAND Data[0]/SPI Flash CLK	
63	110	IOA1	TFT/NAND/SPIF	P	TFT Data[1]/NAND Data[1]/SPI Flash Data[0]	
64	111	IOA2	TFT/NAND/SPIF	P	TFT Data[2]/NAND Data[2]/SPI Flash Data[1]	
1	112	IOA3	TFT/NAND/SPIF	P	TFT Data[3]/NAND Data[3]/SPI Flash Data[2]	

Note: AO: Analog Output, AI: Analog Input

4.1. Package Pin Sequence

LQFP64 Package Top View



5. FUNCTIONAL DESCRIPTIONS

5.1. CPU

The GPEL3101A, capable of running up to 96MHz, integrates the ARM7TDMI CPU with Embedded JTAG ICE and Cache Controller, which supports 8K-byte unified ID-cache and 136K-byte internal SRAM when WMA is disabled. When Cache is enabled, any CPU's R/W will be fetched to the cache instead of external memory to enhance CPU performance. In addition, the internal SRAM bus, I/O bus and cache bus are separated to maximize CPU bus bandwidth.

5.2. Memory

5.2.1. Internal SRAM

The 136K-byte internal SRAM is generally treated as program's stack if WMA is disabled. There is a dedicated 128KB SRAM if WMA is enabled. It can also be accessed by other masters, for example, DMA or USB to reduce external memory bandwidth.

5.2.2. External memory

GPEL3101A also supports up to two SPI Flash and NAND Flash.

5.3. PLL, Clock, Power Mod

5.3.1. PLL (Phase Lock Loop)

There is a PLL embedded in GPEL3101A, the PLL capable of pumping up to 216MHz. The output frequency of fast PLL is programmable and is ranged from 24MHz ~ 216MHz. (6MHz per step)

5.3.2. System clock

One of the following system clocks can be selected via register configuration: 32768Hz, 12MHz or 216MHz (determined by fast PLL's output frequency). Furthermore, a clock divider is provided to reduce power consumption (The divisor is up to 128). The max system clock is 96MHz.

5.4. Power Savings Mode

The GPEL3101A features four power saving modes to extend power life - Normal, Wait, Halt, and Sleep.

Mode	CPU	System	RTC	After wakeup
Normal	ON	ON	ON	-
Wait	OFF	ON	ON	Next Instruction
Halt	OFF	OFF	ON	Reset CPU or not
Sleep	OFF	OFF	OFF	Reset System

Entering the Wait/Halt/Sleep mode is done by writing designated value to designated port. The wake-up source can be interrupt, Time Base, RTC, EXT INT, UART RX.

5.5. Video Input Interface

The GPEL3101A supports video input from sensor or TV decoder. The maximum input resolution is 4095 x 4095. A built-in scalar can be used to scale input data from arbitrary resolution to VGA or QVGA mode. A motion detecting engine is able to recognize the interactive with sensor input. The video-in interface supports CCIR601/CCIR656 format with YUV format. The output format is frame-based and the input frame rate does not need to synchronize with GPEL3101A system clock.

5.6. Video Output Interface

5.6.1. TFT-LCD interface

The GPEL3101A supports TFT-LCD controller with resolution up to 1024x768. The LCD/LCM interface includes serial delta RGB, serial stripe RGB, CPU (MPU / i80) type, CCIR601/CCIR656.

5.7. Sound Process Unit

An 8-channel sound processing unit (SPU) is embedded for sound signal processing. Each channel in this SPU can perform ADPCM/ PCM decode, volume multiply and left/right channel mute control. The SPU also supports automatic zero-crossing concatenate function.

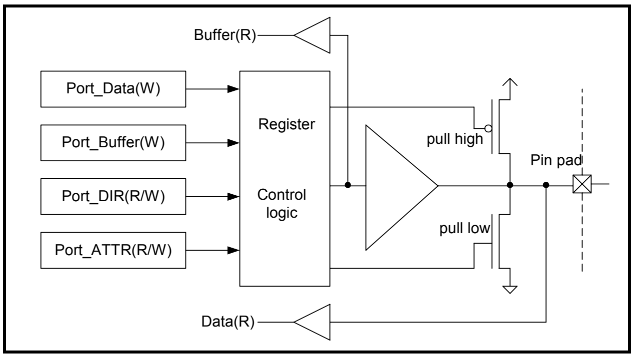
5.8. Interrupt

The GPEL3101A has 25 IRQ (Interrupt request) sources. The priorities of 25 IRQ sources can be configured by programmers.

5.9. I/O

5.9.1. GPIO

GPEL3101A has five I/O ports - IOA, IOB, IOC, IOD and IOE. Each I/O pin has its normal function and is described in the signal description section. When the normal function of the I/O is disabled, it will switch to GPIO function automatically. The following diagram is a GPIO schematic.



5.10. Timer / Counter

Six 16-bit timers/counters are designed in GPEL3101A: TimerA, TimerB, TimerC, TimerD, TimerE, and TimerF. The clock source of each timer can be set individually. For TimerA to TimerD, an INT will be sent to CPU when timer overflow occurs. Besides, Comparison and PWM functions are also provided by TimerA/TimerB/TimerC.

Clock Source A	Clock Source B
Fosc/2	2048Hz
Fosc/256	1024Hz
32768Hz	256Hz
8192Hz	Time Base B
4096Hz	Time Base A
1	0
Another Timer	1
INT1	INT2
CSI_HSYNC	-
CSI_VSYNC	-
AD_I2S_MCLK	-
DA_I2S_MCLK	-

The GPEL3101A also features a Time Base controller to generate slow and precise interrupts from 32768Hz crystal. The following table shows the available Time Base.

TimeBase A	TimeBase B	TimeBase C
--	8Hz	128Hz
1Hz	16Hz	256Hz
2Hz	32Hz	512Hz
4Hz	64Hz	1024Hz

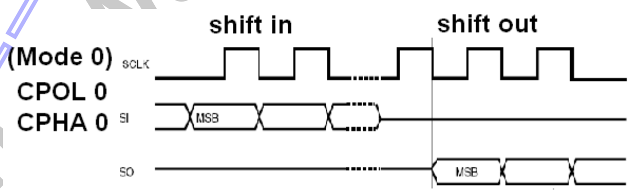
5.11. Watchdog

The purpose of watchdog is to monitor whether or not the system is operating normally. Within a certain period, watchdog must be cleared; otherwise, CPU assumes the program has been running in an abnormal condition. As a result, the CPU will reset the system to the initial state and start running the program all over again. In GPEL3101A, the clear period is software programmable. If watchdog is cleared before the period expires, the system will not be reset.

5.12. Serial Interface

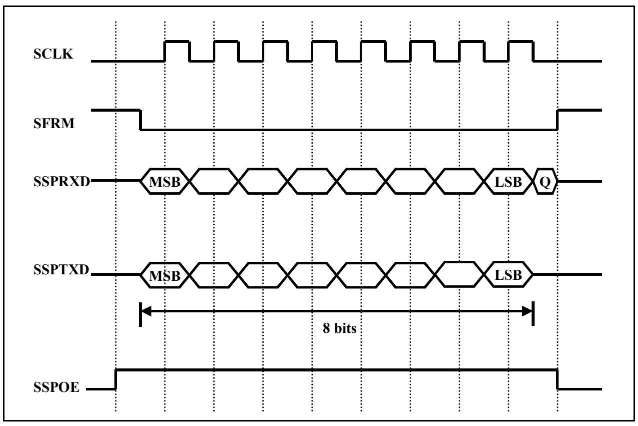
5.12.1. SPI Flash Interface

The SPI Flash Interface is a master interface that enables synchronous serial communications with slave SPI Flash. Only mode 0 is supported and the interface can also be configured as traditional SPI. When configured as traditional SPI, the interface is operated via 4 pins – CSN/SCLK/TX/RX; when configured as SPI Flash Interface, the interface is operated via 6 pins – CSN/ SCLK/SIO_0/ SIO_1/ SIO_2/ SIO_3 while 1x/ 2x/ 4x-mode are supported. When configured as SPI Flash Interface, the interface enables automatic program/read data into/from SPI flash. The command sequences include 1-byte command, 3- or 4-byte address and 0- to 15-byte dummy cycles. Datum is programmed or read following command sequences. When configured as SPI Flash Interface, with adequate setting, executable binary file can be programmed into SPI flash and then GPEL3101A can directly run with codes in SPI flash.

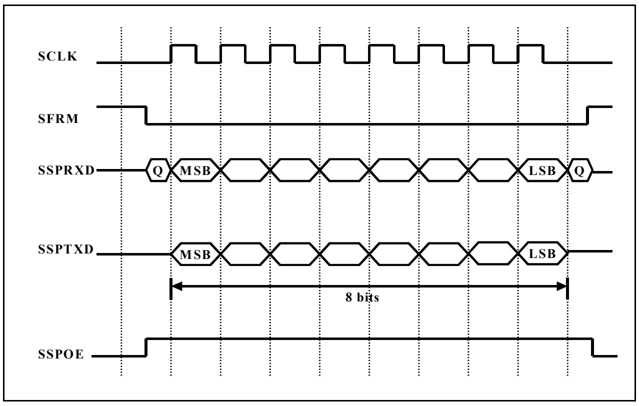


5.12.2. Serial Peripheral Interface (SPI)

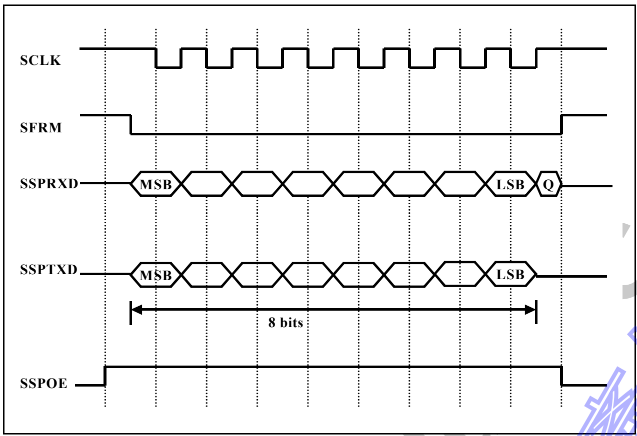
The SPI interface is a master/slave interface that enables synchronous serial communication with slave/master peripherals. Two 8-byte FIFOs are used for transmitting and receiving functions. Four types of timings are supported and shown in the following diagram.



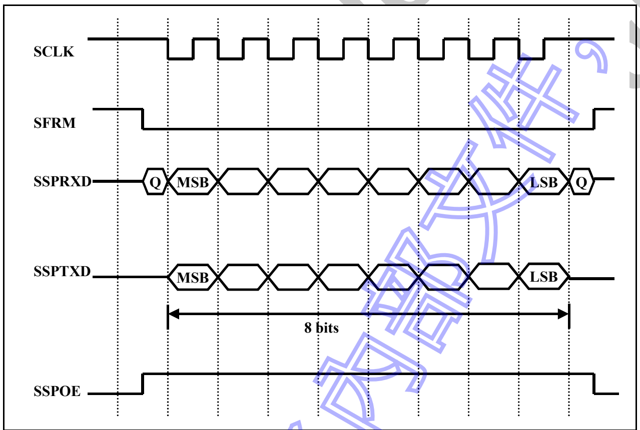
SPO = 0, SPH = 0, only this mode is supported in SPI slave mode.



SPO = 0, SPH = 1



SPO = 1, SPH = 0



SPO = 1, SPH = 1

5.12.3. UART function with smart card interface

The UART controller inside the GPEL3101A supports baud rate up to 1.8432MHz (UART). There are two dedicated 16-byte FIFOs. One is used to prevent the data loss when receiving data and the other is used to transmit data. DMA transfer is available for both transmitting and receiving operations. The UART controller can be configured as smart card interface.(ISO7816).

5.12.4. USB2.0 Mini-host/Device function

The GPEL3101A has USB2.0 mini-host and device function, compatible with USB 1.1 and USB 2.0 high speed standards. The mini-host and device function is not allowed to be active at the same time. A USB transceiver is built-in for both host and device functions. A FIFO with size of 1024x8 is used for bulk-in and bulk-out transfer, a FIFO with size of 192 x 8 is used for audio ISO IN/OUT, a FIFO with size of 512x8 is used for video ISO IN and a 64-byte FIFO is used for control pipe transfer. Interrupt IN pipes are also supported. The DMA transfer is enabled for bulk-in/out to maximize the transfer performance.

5.13. DMA Controller

The GPEL3101A provides four DMA channels and each channel can be individually configured in I/O to MEM, MEM to I/O or MEM to MEM mode.

5.14. Secure Disk / Multi-Media Card Controller

The SD/MMC controller is compatible with MMC system specification version 2.3, SD Memory Card specification 2.0, SDHC and SDIO card interface. The controller supports automatically CRC generation and check, 1-bit and 4-bit transfer, interrupt generation when buffer empty/full, DMA transfer for page read/write. There are two SD card controllers inside the chip.

5.15. Real Time Clock (RTC)

The RTC block supports independent power supply, and also offers the alarm function, schedule function, and day/ hour/ minute/ second/ half-second interrupt function.

5.16. Analog Control

5.16.1. DAC control

A 16-bit stereo DAC (2-channel) is embedded for both left and right channels. A 16x16 FIFO is used to prevent the sound glitch when CPU is busy. The left and right channels do not need to have the same sample rate. A single DMA channel can utilize the stereo playback.

5.16.2. Audio Amplifier

A mono class AB audio amplifier is built-in. It can drive an 8Ω speaker directly.

5.16.3. ADC control

A 12-bit ADC is embedded in GPEL3101A for general purpose application. The ADC has two inputs which can be selected by software programming with max. 62.5KHz sample rate. It also provides an independent MIC channel with PGA function (Programmable Gain Amplifier) for voice recording application.

6. ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Rating

Rating	Symbol	Value	Unit
Supply Voltage 1	DC5V V50_AMP	-0.3 to 5.5	V
Supply Voltage 2	V33IO V33_ADC V33_DA16 V33IO_REG AVDDTX AVDDRX V33_CLKGEN	-0.3 to 4.0	V
Supply Voltage 3	V12 V12_REG	-0.3 to 1.44	V
Supply Voltage 4	V33_RTC	-0.3 to 4.2	V
Input Voltage	V_{IN}	-0.3 to 4.0	V
Operating Temperature	T_A	-40~70	℃
Storage Temperature	T_{STG}	-40 to +150	℃

6.2. DC Characteristics

Characteristic	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
Operating Voltage 1	DC5V V50_AMP	3.0	3.6	5.5	V	-
Operating Voltage 2	V33IO V33_ADC V33_DA16 V33IO_REG V33_RTC AVDDTX AVDDRX V33_CLKGEN	2.7	3.3	3.6	V	-
Operating Voltage 3	V12 V12_REG	1.08	1.2	1.32	V	-
Operating Voltage 4	V33_RTC	1.4	3.3	4.0	V	-
Operating Current	I_{OP}	-	70	-	mA	System clock=96MHz, PLL enable, all IP ON, USB OFF
Power Down Current (RTC Only)	I_{PD}	-	15	-	µA	-
High Input Voltage	V_{IH}	2.0	-	DVDD33	V	-
Low Input Voltage	V_{IL}	VSS	-	0.8	V	-
Crystal Frequency 1	-	-	32768	-	Hz	-
Crystal Frequency 2	$F_{CRYSTAL}$	-	12	-	MHz	-
System Clock	F_{SYS}	256Hz[1]	-	96	MHz	-
Stop mode operation current PLL=192MHz	Istop1	-	30	-	mA	DC5V=5.5V, System clock=48MHz, PLL=192MHz, all IP on, USB off

Characteristic	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
System clock=48MHz OTP=48MHz	Istop2	-	14.5	-	mA	DC5V=5.5V, PLL=192MHz, all IP off, USB off
	Istop3	-	28	-	mA	DC5V=3V, System clock=48MHz, PLL=192MHz, all IP on, USB off
	Istop4	-	13	-	mA	DC5V=3V, PLL=192MHz, all IP on, USB off
Stop mode operation current PLL=192MHz System clock=96MHz OTP=48MHz	Istop1	-	42.5	-	mA	DC5V=5.5V, System clock=96MHz, PLL=192MHz, all IP on, USB off
	Istop2	-	14.5	-	mA	DC5V=5.5V, PLL=192MHz, all IP off, USB off
	Istop3	-	40.5	-	mA	DC5V=3V, System clock=96MHz, PLL=192MHz, all IP on, USB off
	Istop4	-	13	-	mA	DC5V=3V, PLL=192MHz, all IP on, USB off

Note1: By setting clock divider and changing system clock to 32768Hz mode.
Note2: When USB function is enabled, the minimum voltage of DVCC33 is 3.0V.

6.3. Audio DAC Characteristics

Characteristic	Limits			Unit	Condition
	Min.	Typ.	Max.		
Resolution	-	-	16	Bit	-
Full Scale Output Voltage	-	0.6*V33_DA	-	Vp-p	-
THD+N (Fin = 0.997kHz)	-	0.1	-	%	-
Dynamic Range	85	90	-	dB	Fin=0.997KHz w/ -60dB output loading=125 ohm
Output Loading	125	-	-	ohm	-
Frequency Response	20	-	19200	Hz	-

6.4. Audio Amplifier Characteristics

Characteristic	Limits			Unit	Condition
	Min.	Typ.	Max.		
Full Scale Output Voltage	-	5.3	-	Vp-p	-
THD+N (4.2V@0.5W)	-	0.37	-	%	-
Noise at No Signal	-	80	-	dBv	-
Dynamic Range	-	80	-	dBv	-

6.5. ADC Characteristics

Characteristics	Symbol	Limits			Unit
		Min.	Typ.	Max.	
SAR ADC Input Voltage Range	V33_AD	3.0	-	3.6	V
Resolution of ADC	RESO	-	12	-	bits

Characteristics	Symbol	Limits			Unit
		Min.	Typ.	Max.	
Signal-to-Noise Plus Distortion of ADC from Line in	SINAD (Note 1)	-	55	-	dB
Effective Number of Bit	ENOB (Note 2)	-	8.9	-	bits
Integral Non-Linearity of ADC	INL(Note 3)	-	3.7~-2.6	-	LSB
Differential Non-Linearity of ADC	DNL (Note 3)	-	0.34~-1	-	LSB
No Missing Code		-	10	-	bits
AD Conversion Rate=ADCCLK/16	F_{CONV}	-	-	62.5K	Hz

Note1: The SINAD testing condition at VINLp-p = 0.8 * V33_AD, F_{CONV} = 62.5KHz, Fin = 1.0KHz Sine waves at V33_AD = 3.0V from the ADC input.
Note2: ENOB = (SINAD - 1.76) / 6.02.
Note3: LSB means Least Significant Bit (at 12 bits resolution). With V33_AD = 3.3V, 1LSB = 3.3V / 2^12 =3.01mV.

6.6. 4.2V-to-3.3V Regulator Characteristics

Characteristics	Symbol	Limits			Unit
		Min.	Typ.	Max.	
Input Voltage	VREGI	3.3	3.6	5.5	V
Maximum Current Output	IREGO	-	-	300	mA
Output Voltage	VREGO	3.0	3.3	-	V
Standby Current	IREGS	-	2	-	uA

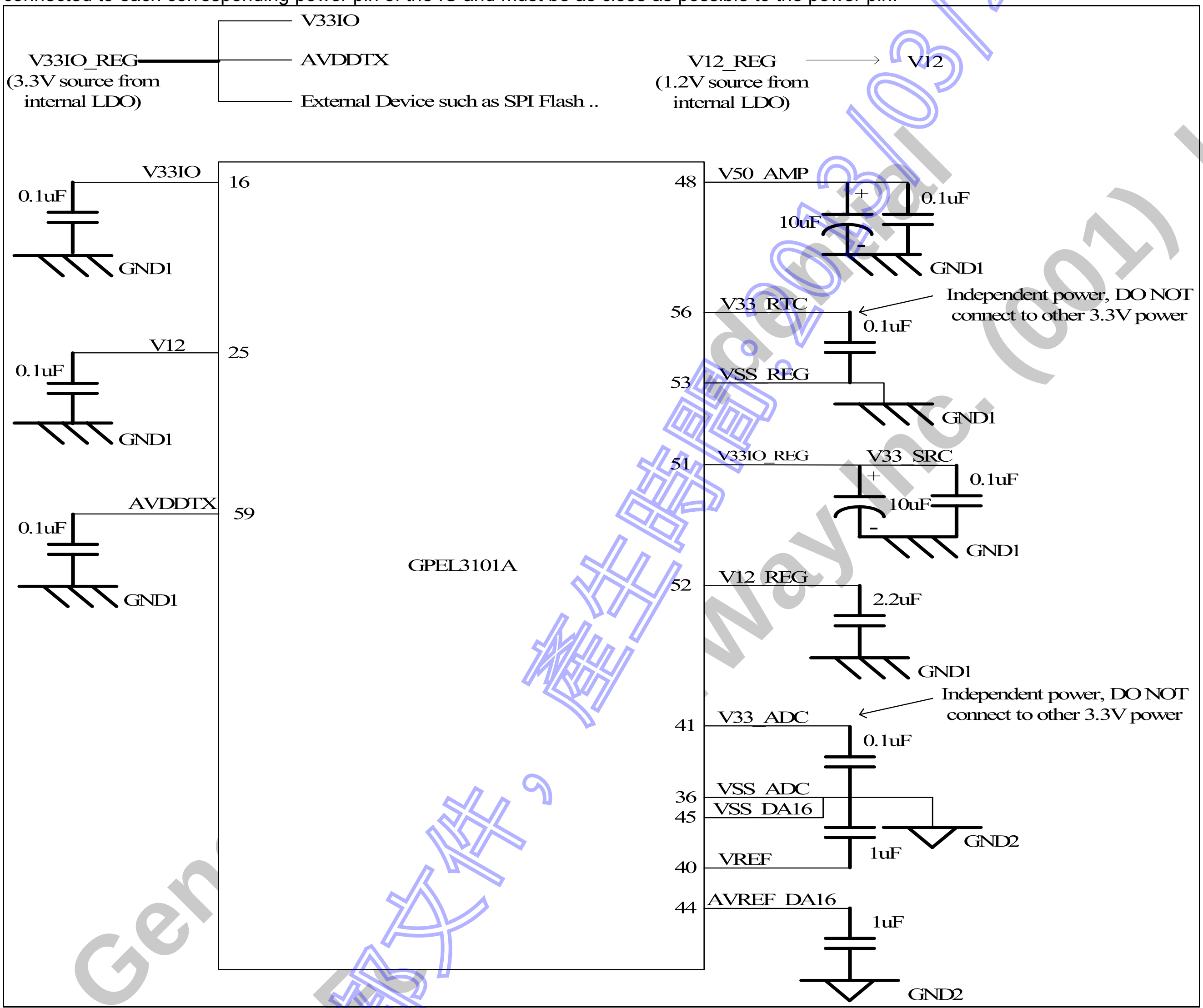
6.7. 3.3V-to-1.2V Regulator Characteristics

Characteristics	Symbol	Limits			Unit
		Min.	Typ.	Max.	
Input Voltage	VREGI	2.7	3.3	3.6	V
Maximum Current Output	IREGO	-	-	150	mA
Output Voltage	VREGO	-	1.2	-	V
Standby Current	IREGS	-	2	-	uA

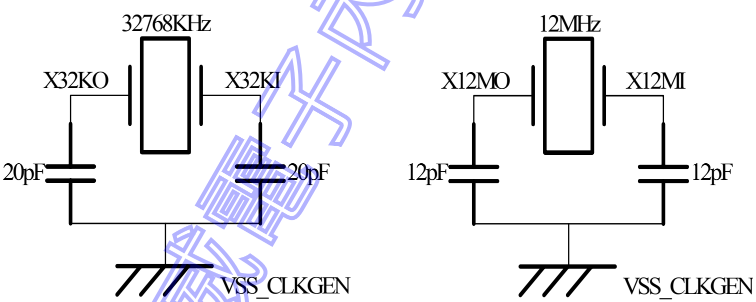
7. RECOMMENDED BOARD LAYOUT

7.1. Power and Ground

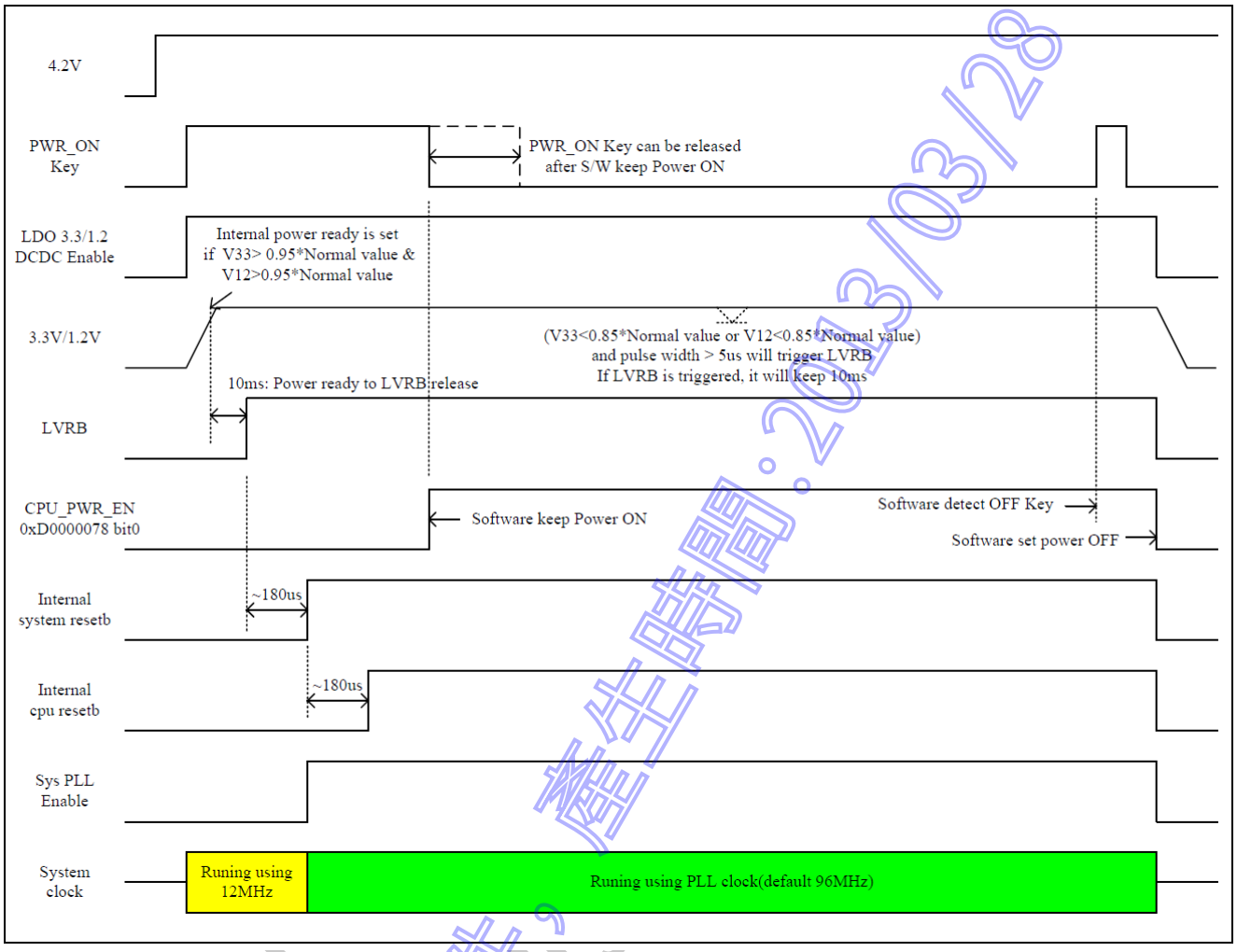
All power and ground pins are connected as in the following diagram for general application. The decoupling capacitor should be connected to each corresponding power pin of the IC and must be as close as possible to the power pin.



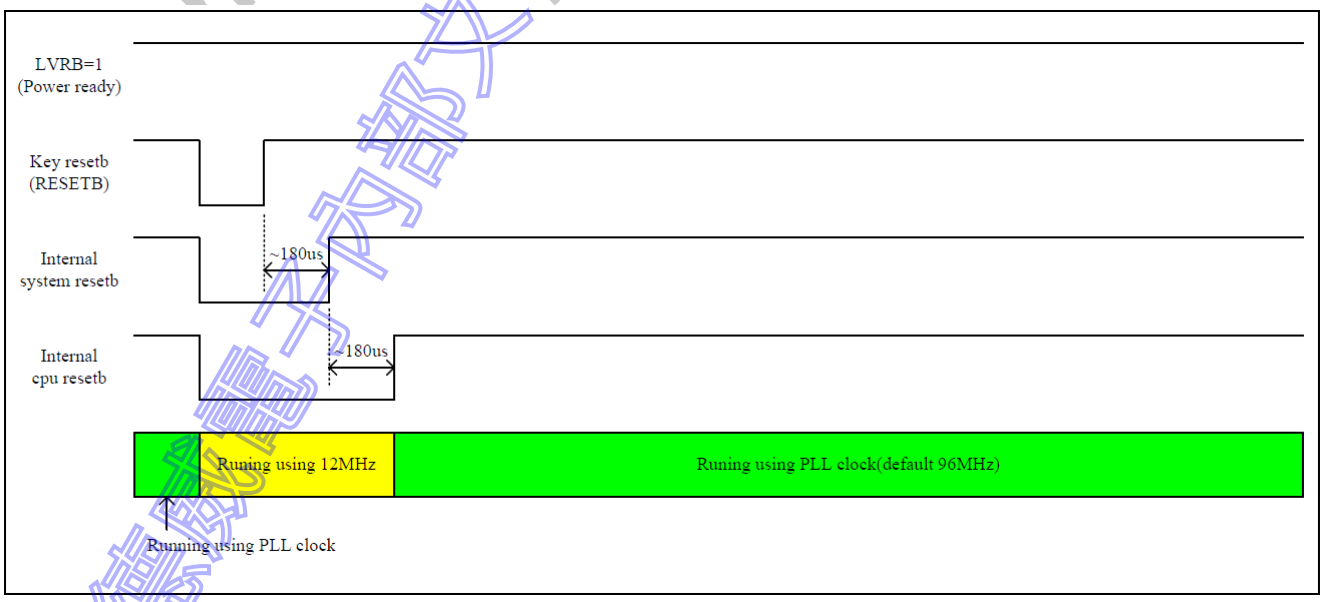
7.2. Crystal and PLL



8. POWER ON/OFF SEQUENCE



9. KEY RESET TIMING



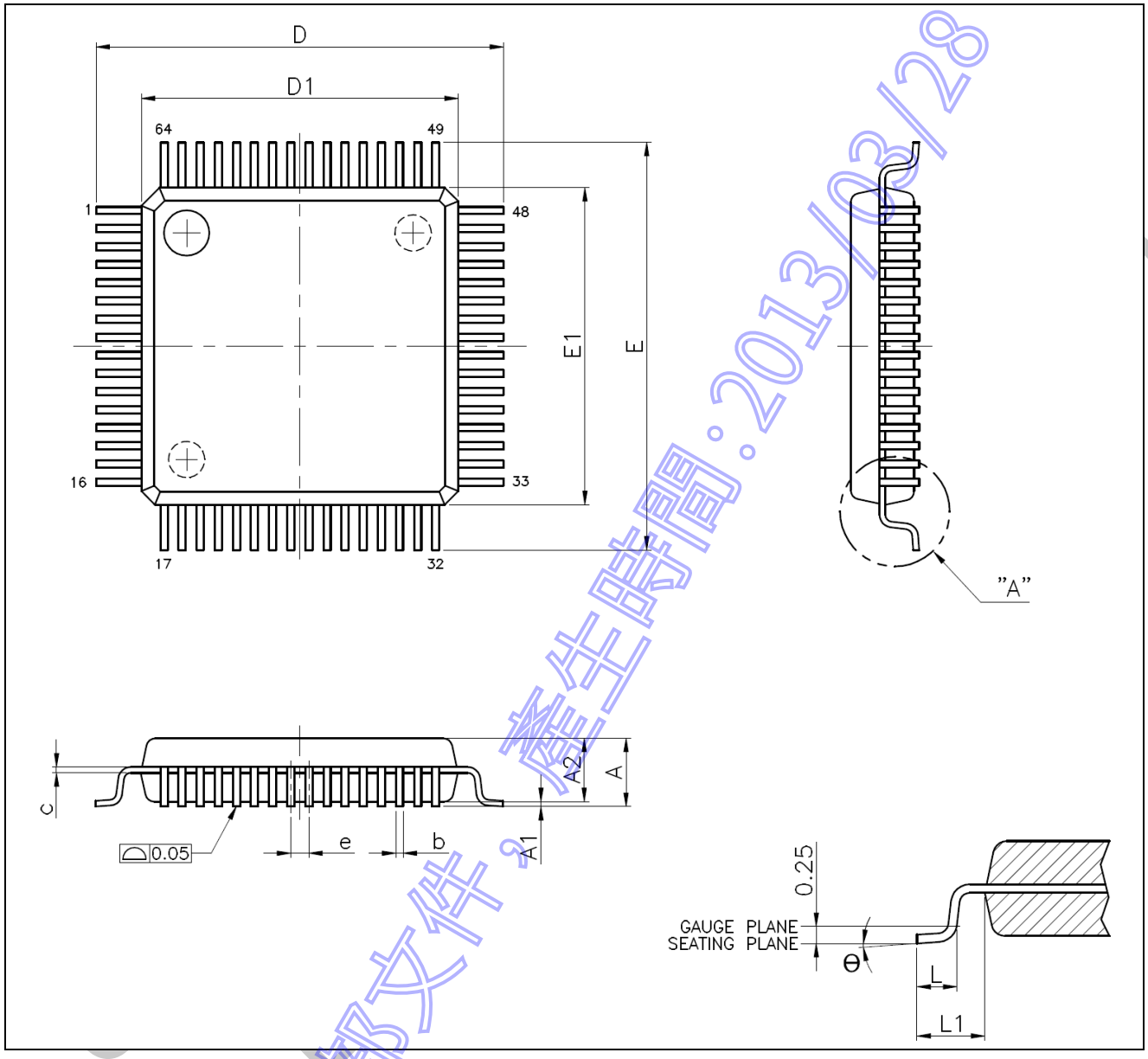
10. PACKAGE/PAD LOCATIONS

10.1. Ordering Information

Product Number	Package Type
GPEL3101A-NnnV-QL09x	Halogen Free Package

Note1: Code number is assigned for customer.
Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).
Note3: Package form number (x = 1 - 9, serial number).

10.2. Package Information



Symbols	Min.	Nom.	Max.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
c	0.09	-	0.20
D	9.00 BSC		
D1	7.00 BSC		
e	0.40 BSC		
E	9.00 BSC		
E1	7.00 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

11. DISCLAIMER

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12. REVISION HISTORY

Date	Revision #	Description	Page
Mar 12, 2013	0.3	1. Internal SRAM 136KB when WMA is disable 2. 12-bit ADC 3. Add Power On/Off sequence 4. Add Key reset timing	
Nov 12, 2012	0.2	1. Modify the total number of GPIOs. 2. Modify electrical specifications. 3. Modify “7. Recommended Board Layout”. 4. Modify ordering information, chip form is not available. 5. Modify 8.2. Package Information	4 11-13 14 15 16
Aug 24, 2012	0.1	Preliminary version.	18